Appln. No.: 10/743,385

Preliminary Amendment dated March 17, 2004

Amendments to the Specification:

Please amend the title of the application as follows:

SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE WITH ERASABLE AND

PROGRAMMABLE FUSE MEMORY

Please replace the entire Abstract of the Disclosure with the following amended Abstract of the

Disclosure:

A semiconductor integrated circuit device includes fuse cells arranged at a fuse cell array, a fuse

cell data program and erase circuit, a fuse cell data control circuit, and fuse data latch circuits.

The fuse cells include erasable and programmable nonvolatile memory cells. The fuse cell data

program and erase circuit programs fuse data to the memory cells and erases the fuse data from

the memory cells. The fuse cell data control circuit controls read out timing of the fuse data

stored in the memory cells based on a signal generated upon detection of power-on. The fuse

data latch circuits latch the fuse data read out from the memory cells.

Please replace paragraph [22] with the following amended paragraph:

[22] A semiconductor integrated circuit device according to an aspect of the present invention

comprises: a fuse cell array; fuse cells arranged at the fuse cell array, the fuse cells including

erasable and programmable nonvolatile memory cells; a fuse cell data program and erase circuit

which programs fuse data to the erasable and programmable nonvolatile memory cells and erases

the fuse data from the erasable and programmable nonvolatile memory cells; a fuse cell data

control circuit which controls read out timing of the fuse data stored in the erasable and

programmable nonvolatile memory cells, based on a first signal generated upon detection of

power-on; and fuse data latch circuits which latch the fuse data read out from the erasable and

programmable nonvolatile memory cells.

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